BSTZ No. 042390.P11362
Express Mail No. EL802872991US

UNITED STATES PATENT APPLICATION

FOR

CREATION OF HIGH MOBILITY CHANNELS IN THIN-BODY SOI DEVICES

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FIELD OF THE INVENTION

[0001] This invention relates to a method for fabricating strain on a wafer. In particular, the invention relates to a method for fabricating strain on a silicon-on-insulator (SOI) wafer.

BACKGROUND OF THE INVENTION

[0002] The mobility of the carriers in a device is directly related to the its current. The higher the current the faster the device is operated. Devices can be built as bulk devices, devices on silicon on insulator (SOI) or any other types. Each type has its own characteristics that make it attractive. As these devices are scaled down, one of the characteristics that may be of interest is the speed of metal oxide semiconductor (MOS) transistors. One way to make a speedier transistor is to create a thinner gate oxide and therefore create more capacitance, which results more charge. Another way is to create a high mobility channel.

[0003] To have a high mobility channel is to have high carriers mobility in the device. Straining the channel region of the MOS devices produces higher mobility of the carriers since tensile strained silicon causes increases in the mobility of both electrons and holes. Higher the mobility of these carriers means higher current; therefore faster devices or faster chips.

[0004] The method of growing strained silicon film on top of Silicon Germanium (SiGe) layer in bulk devices (e.g., silicon substrate) is standard and is well known in the art. Growing strained silicon film onto silicon-on-insulator wafer, however, is difficult since it would thicken the active silicon layer on the SOI beyond the range of useful interest.

[0005] A method of fabrication of a thin film strained silicon layer on an oxide substrate (i.e., thin body SOI) is described.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The features and advantages of the present invention will become apparent from the following detailed description of the present invention in which:

[0007] Figure 1 is a diagram illustrating a sectional view of a wafer having a stack structure of a conventional substrate with a relaxed layer and a strained layer.

[0008] Figure 2 is a diagram illustrating Figure 1 with an implantation of hydrogen onto the substrate to create stress according to one embodiment of the invention.

[0009] Figure 3 is a diagram illustrating Figure 2 with a deposition of oxide layer onto the strained layer according of one embodiment of the invention.

[0010] Figure 4 is a diagram illustrating Figure 3 brought in contact with oxidized silicon wafer according to one embodiment of the invention.

[0011] Figure 5 is a diagram illustrating Figure 4 having a heat treatment to bond the two wafers according to one embodiment of the invention.

[0012] Figure 6 is a diagram illustrating Figure 5 with further heat treatment to transfers the strained layer to the oxidized wafer according to one embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0013] In the following, for purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that theses specific details are not required in order to practice the present invention.

[0014] Figure 1 is a diagram illustrating a sectional view of a wafer having a stack structure of a conventional substrate with a strained silicon layer. The wafer 100 may includes heteroepitaxial layers of a starting silicon platform (e.g., substrate) 101, a silicon germanium (SiGe) alloy graded relaxed buffer layer 102, and a strained silicon layer 104.

[0015] The relaxed SiGe layer 102 is formed upon or deposited on top the silicon substrate 101. The strained silicon layer 104 is then formed on the relaxed SiGe layer 102. In one embodiment, the relaxed SiGe layer 102, and the strained silicon layer 104 are formed by an epitaxial growth process. In other words, the process includes epitaxial growth of relaxed SiGe on the silicon wafer 101 to create the relaxed SiGe layer 102, epitaxial growth of a thin silicon film on the stack structure of the silicon wafer 101 to create the strained silicon film 104. The relaxed SiGe layer has the thickness in the range of approximately from 0.1 to 3.0. It is contemplated that the forming of these layers in the stack structure may be done in any other process other than the epitaxial growth process.

[0016] Figure 2 is a diagram illustrating Figure 1 with an implantation of an ion onto the substrate to create stress according to one embodiment of the invention. With the stack structure of the silicon wafer 101 discussed in Figure 1, in one embodiment, hydrogen ions are implanted into the silicon wafer 101 to create stress on the wafer. The implanting of the hydrogen ions is performed to result in an embrittled region in one of the layers in the stack structure of the wafer 101. In other words, the stress creates an embrittled region on one of the layers in the stack structure of the silicon wafer 101. The location of the embrittled region depends of the energy used in the implanting process. The energy level used in the implanting process is in the range from approximately 1 keV to 20 keV and the dose used is in the range from approximately 1E116/cm^3 to 1E18/cm^3. It is contemplated that the other type of ions

may be used in place of hydrogen in the implanting process to create the embrittled region in the wafer 101.

[0017] Figure 3 is a diagram illustrating Figure 2 with a deposition of oxide layer onto the strained silicon layer 104 according of one embodiment of the invention. A thin oxide layer 301 is deposited (i.e., grown) onto the strained silicon layer 104. The deposition of oxide layer 301 on the strained silicon film 104 is used for adhesion purpose. After the deposition process, a plasma treatment is applied on the surface of the silicon wafer 101. This plasma treatment is performed at low temperatures to ensure the bonding of the stack structures. The temperature may be in the range of approximately from 100 °C to 400 °C.

[0018] Figure 4 is a diagram illustrating Figure 3 brought into contact with the SOI substrate wafer (e.g., oxidized wafer) 401 according to one embodiment of the invention. The silicon wafer 101 as described in Figure 3 is brought into contact with the SOI substrate wafer 401.

[0019] The oxidized wafer 401 is a SOI substrate wafer and is plasma treated before making contact with the silicon wafer 101. The strained silicon film 104 is later transferred to this oxidized wafer 401. Any well-known process may fabricate the SOI substrate 401.

[0020] Figure 5 is a diagram illustrating Figure 4 having a heat treatment to bond the two wafers according to one embodiment of the invention. Once the silicon wafer 101 and the oxidized wafer 401 are in contact, a heat treatment is performed on the two contacted wafers. The temperature used in the heat treatment is in the range of approximately 100 °C to 300 °C. This heat treatment results in the bonding of the two wafers 101 and 401. In other words, the heat treatment on the two wafers causes the SiO_2 dangling bond on both of the wafer surfaces to bond to each other. It is noted that this technique is also well known in the art.

[0021] Figure 6 is a diagram illustrating Figure 5 with further heat treatment to transfer the strained layer to the oxidized wafer according to one embodiment of the invention. After the lower heat treatment to result the bonding of silicon wafer 101 and oxidized wafer 401, higher temperature heat treatment is applied. This temperature used in this further heat treatment ranges from approximately 400 °C to 600 ° C. The higher temperature heat treatment results in the bonding of surface 104 to wafer 101at

the SiO2 interface 601. The further heat treatment also results in the separation of the two wafers at the embrittled region (described in Figure 2). After the further heat treatment, the two wafers 101 and 401 are delaminated along the embrittled implanted region (i.e., H-implanted SiGe region). This effectively separates the two wafers and the strained silicon film 104 is transferred to the SOI-like wafer 401. In one embodiment, the embrittled region resides on the relaxed SiGe layer 102. When the two wafers 101 and 401separate, the strained silicon layer 104 and the part of the relaxed SiGe layer 102 are transferred to the SOI wafer 401. Part of relaxed SiGe layer 102 is then etched off to result the wafer 401 with the strained silicon layer 104 on top of the SiO_2 layer. This results in the transfer of the strained silicon layer 104 to the SOI wafer 401(e.g., oxidized wafer 401). It is contemplated that the etching may be wet or plasma etching; however, wet etching is used to better remove the entire SiGe residue on the strained silicon film.

[0022] In one embodiment where there is no implanting step (i.e., hydrogen implant), the embrittled region is not formed. The strained silicon layer 103 is transferred to the SOI wafer 401 by a bonded-etchback process on the silicon wafer 101 and the strained SiGe 103. This gives the strained silicon film on the SOI wafer 401.

[0023] While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the invention, which are apparent to persons skilled in the art to which the invention pertains are deemed to lie within the spirit and scope of the invention.